METHOD OF FORMING A SEMICONDUCTOR LASER CHIP HAVING A MARKER

Background of the Invention

The present invention relates to a method of forming a semiconductor chip, and more specifically to formation of laser chip markers for passive alignment.

The passive alignment has been described in "Synonymous With Alignment-Optical Packaging", Journal of Japan Institute of Electronics Packaging, Vol. 13, No. 1 (1988), pp 54-56. While a visual type, a mechanical type, and a flip-chip type have been introduced for the passive alignment in the present Journal, the present invention relates to the visual type.

According to the above-described document, the visual type passive alignment is equivalent to one wherein a chip mounter adopted in die bonding of electronic components such as an LSI chip is made high in accuracy. Both a mounting board and an optical chip are provided with eye-alignment markers, and both positions thereof are detected by image recognition. Thereafter, a stage for holding the optical chip is moved to a predetermined position and fixed thereat.

The markers provided on the chip are respectively made up of a metal formed on a silicon oxide film on the surface of the chip. In general, the markers are provided plural per chip and respectively take easy-to-visually

recognize shapes such as round shapes.

Since, however, the markers on the chip are formed on the silicon oxide film, they might produce imperfections that the metal surfaces of the markers are flawed, the shapes thereof are reduced or become large in reverse, or the markers are deformed and peeled as the case may be. When the imperfections occur in such markers, a problem arises in that the chip cannot be packaged on a mounting board due to passive alignment even if the chip per se is a non-defective item free of any problem in terms of its characteristic.

Summary of the Invention

The present invention may provide a method for forming a semiconductor chip having chip markers with no flaws and free of the occurrence of deformation and peeling.

According to the present invention, chip markers are simultaneously formed of the same material as electrode lines for ohmic contacts. The so-formed markers are covered with a silicon oxide film for current narrowing.

According to the present invention as well, the chip markers are also formed as patterns void of the silicon oxide film for current narrowing.

Brief Description of the Drawings

While the specification concludes with claims particularly pointing out and distinctly claiming the subject matter which is regarded as the invention, it is believed that the invention, the objects and features of the invention and further objects, features and advantages thereof will be better understood from the following description taken in connection with the accompanying drawings in which:

Figs. 1(A) through 1(D) are respectively diagrams showing a method of forming a semiconductor chip, according to a first embodiment of the present invention; and

Figs. 2(A) through 2(D) are respectively diagrams illustrating a method of forming a semiconductor chip, according to a second embodiment of the present invention.

Detailed Description of the Preferred Embodiments

Preferred embodiments of the present invention will hereinafter be described in detail with reference to the accompanying drawings.

Figs. 1(A) through 1(D) are forming process diagrams of a semiconductor chip, showing a first embodiment of the present invention.

As shown in Fig. 1(A), ohmic contact electrode lines 102 and markers 103 are first formed on the junction side of an InP substrate 101 having an active layer and a block layer. The ohmic contact electrode

lines 102 and the markers 103 are respectively composed of AuZu and simultaneously formed by lift-off. Thereafter, sintering is performed to ensure ohmic contacts between the ohmic contact electrode lines 102 and the InP substrate 101.

Next, as shown in Fig. 1(B), the InP substrate 101 is etched to form W channels 104. Thereafter, a silicon oxide film 105 for current narrowing is formed over the whole surface. Further, afterwards, the silicon oxide film 105 is etched to open line patterns 106 of electrode contact portions on their corresponding ohmic contact electrode lines 102.

As shown in Fig. 1(C), mounting electrodes 107 are respectively formed on the line patterns 106 of the electrode contact portions so as to have electrical connections with the ohmic contact electrode lines 102. Portions formed as peripheral portions when the InP substrate 101 is diced into chip single bodies, are removed from the silicon oxide film 105. Thereafter, lines 108 for cleaving the silicon oxide film are formed on the InP substrate 101. Further, the InP substrate 101 is polished so as to reach 100μm, so that unillustrated back electrodes are formed.

Finally, as shown in Fig. 1(D), bar cleavage is performed along the cleavage lines 108 to fractionalize the InP substrate 101 into semiconductor chip single bodies 110. Thereafter, end-face coats 109 are processed

so as to be applied to the semiconductor chip single bodies 110, whereby each individual semiconductor chip 101 is formed.

According to the first embodiment of the present invention, as described above, since the laser chip markers 103 for passive alignment are covered with the silicon oxide film 105 for current narrowing, flaws in metal electrode portions of the markers 103, and marker peeling can be prevented from occurring.

Forming the markers 103 by the same mask as the ohmic contact electrode line 102 on the active layer makes it possible to hold the active layer and the markers 103 with high position accuracy. Also using the lift-off enables prevention of failures in the size and shape of each marker 103 due to variations in metal etching.

A second embodiment of the present invention will next be explained with reference to Figs. 2(A) through 2(D). Figs. 2(A) through 2(D) are forming process diagrams of a semiconductor chip, showing the second embodiment of the present invention.

As shown in Fig. 2(A), ohmic contact electrode lines 202 are first formed on the junction side of an InP substrate 201 having an active layer and a block layer. The ohmic contact electrode lines 202 are respectively composed of AuZu and formed by lift-off. Thereafter, sintering is performed to ensure ohmic contacts between

the ohmic contact electrode lines 202 and the InP substrate 201.

Next, as shown in Fig. 2(B), the InP substrate 201 is etched to form W channels 203. Thereafter, a silicon oxide film 204 for current narrowing is formed over the whole surface. Further, afterwards, as shown in Fig. 2(C), the silicon oxide film 204 is etched to simultaneously form line patterns 205 of electrode contact portions and markers 206 on their corresponding ohmic contact electrode lines 202. The markers 206 expose the InP substrate 201.

Thereafter, although not shown in the drawing in particular, mounting electrodes are respectively formed on the line patterns 205 of the electrode contact portions so as to have electrical connections with the ohmic contact electrode lines 202 in a manner similar to the first embodiment. Portions formed as peripheral portions when the InP substrate 201 is diced into chip single bodies, are removed from the silicon oxide film 204. Thereafter, lines for cleaving the silicon oxide film are formed on the InP substrate 201. Further, the InP substrate 201 is polished so as to reach 100μm, so that unillustrated back electrodes are formed.

Finally, bar cleavage is performed along the cleavage lines to fractionalize the InP substrate 201 into semiconductor chip single bodies 207. Thereafter, end-face coats are processed so as to be applied to the

semiconductor chip single bodies 207, whereby each individual semiconductor chip is formed.

According to the second embodiment of the present invention, as described above, the silicon oxide film 204 is removed so that the InP substrate 201 is exposed, whereby the markers 206 are formed. It is therefore possible to prevent the occurrence of flaws liable to be formed on a metal, and an imperfection in contrast at a metal portion due to image processing. Further, since the markers 206 are of void patterns, peeling does not occur either.

Since the line patterns 205 of the electrode contact portions and the markers 206 are simultaneously formed on the ohmic contact electrode lines 202, the position accuracy of each marker can be also held high.

When multilayer films are used for a dielectric material such as the silicon oxide film for current narrowing in the first embodiment described above, the markers may be formed between the multilayer films.

In the second embodiment, the markers may be formed by etching simultaneously with the formation of the cleavage lines.

While the present invention has been described with reference to the illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications of the illustrative embodiments, as well as other embodiments of the

invention, will be apparent to those skilled in the art on reference to this description. It is therefore contemplated that the appended claims will cover any such modifications or embodiments as fall within the true scope of the invention.